Amendments to the Claims

1. (original) A photolithographic mask set comprising:

a master mask including a first pattern having features for forming part of a planar circuit, the first pattern including a featureless region disposed therein such that the planar circuit is incomplete; and,

a slave mask including a second pattern having features for completing the planar circuit.

2. (original) A photolithographic mask set according to claim 1, wherein the second pattern is designed to correct systematic errors induced by the master mask.

3. (original) A photolithographic mask set according to claim 1, wherein the second pattern has been experimentally optimized using a plurality of other slave masks.

4. (original) A photolithographic mask set according to claim 1, wherein a perimeter of the featureless region and a perimeter of the slave mask have a same shape and dimensions.

5. (original) A photolithographic mask set according to claim 1, wherein the master mask and the slave mask are written on different regions of a same plate.

6. (original) A photolithographic mask set according to claim 5, wherein the slave mask is written at a periphery of the master mask.

7. (original) A photolithographic mask set according to claim 1, wherein the master mask and the slave mask are written on different plates.

8. (original) A photolithographic mask set according to claim 7, comprising a plurality of other slave masks written on the same plate as the slave mask.

9. (original) A method of fabricating a planar circuit utilizing a photolithographic mask set, the method comprising the steps of:

(a) providing a photolithographic mask set including a master mask and a slave mask, the master mask including a first pattern having features for forming part of the planar circuit and including a featureless region disposed within the first pattern such that the planar circuit is incomplete, the slave mask including a second pattern having features for completing the planar circuit;

(b) using the photolithographic mask set to expose at least part of a substrate;

(c) processing the exposed substrate to fabricate the planar circuit;

(d) analyzing the fabricated planar circuit; and

(e) determining an optimized planar circuit in dependence upon the analysis.

10. (original) A method according to claim 9, comprising the step of fabricating the optimized planar circuit.

11. (original) A method according to claim 9, wherein step (b) comprises:

aligning the master mask above the substrate and exposing the substrate through the master mask; and,

aligning the slave mask above the substrate and exposing the substrate through the slave mask, the slave mask aligned such that features in the second pattern align with corresponding features in the first pattern on the substrate.

12. (original) A method according to claim 9, wherein the planar circuit is a planar lightwave circuit, and wherein step (d) comprises measuring at least one of phase and amplitude errors of the fabricated planar lightwave circuit.

13. (original) A method according to claim 12, wherein step (d) further comprises using the at least one measured error to design at least one correcting slave mask.

14. (original) A method according to claim 13, wherein step (d) further comprises repeating steps (b) though (d) for the at least one correcting slave mask.

15. (original) A method according to claim 9, wherein step (e) comprises calculating a desired modification to the slave mask to modify a property of the planar circuit.

16. (original) A method according to claim 9, wherein step (b) comprises stitching the slave mask to the master mask about a periphery of the featureless region.

17. (original) A method according to claim 13, comprising the step of writing a production mask from data from the master mask and the at least one correcting slave mask.

18. (original) A method according to claim 9, wherein step (b) comprises the step of exposing a resist layer formed on an optical core layer.

19. (original) A planar circuit fabricated from a photolithographic mask set comprising:

a substrate;

a first pattern formed on a layer of the substrate, the first pattern including features for forming part of a planar circuit; and

a second pattern formed on the layer of the substrate, the second pattern disposed within the first pattern and including features for completing the planar circuit,

wherein the second pattern includes at least one modificator section selected for optimizing the planar circuit.

20. (original) A planar circuit according to claim 19, wherein the at least one modificator section is designed for compensating systematic errors produced by the first pattern.

21. (original) A planar circuit according to claim 19, wherein the planar circuit comprises a planar lightwave circuit.

22. (original) A planar circuit according to claim 21, wherein the at least one modificator section includes a plurality of

waveguides that are modified relative to a corresponding plurality of waveguides outside the modificator section.

23. (original) A planar circuit according to claim 22, wherein the modifications comprise at least one expanded width of a waveguide.

24. (original) A planar circuit according to claim 22, wherein the modifications comprise at least one gap within a waveguide.

25. (original) A planar circuit according to claim 22, wherein the modifications comprise at least one lateral offset between a section of a waveguide within the modificator section and a section of the waveguide outside the modificator section.

26. (original) A planar circuit according to claim 22, wherein the modifications comprise at least one of an expanded waveguide width of a waveguide, a gap within a waveguide and a lateral offset between a section of a waveguide within the modificator section and a section of the waveguide outside the modificator section.

27. (original) A planar circuit according to claim 21, wherein the at least one modificator section is designed for changing an optical response of the planar lightwave circuit that is substantially determined by the first pattern.

28. (original) A planar circuit according to claim 21, wherein the at least one modificator section is designed for compensating systematic errors produced by the first pattern.

29. (original) A planar circuit according to claim 21, wherein the planar lightwave circuit comprises an arrayed waveguide

grating having a plurality of waveguides of different lengths arranged in an arc on the substrate.

30. (original) A planar circuit according to claim 29, wherein the at least one modificator section substantially bisects the arc.

31. (original) A planar circuit according to claim 30, wherein the at least one modificator section is a rectangular straight region.

32. (original) A planar circuit according to claim 30, wherein the at least one modificator section includes an elliptical region.

33. (original) A planar circuit according to claim 21, wherein the at least one modificator section is designed for compensating variations in refractive index across the substrate.

34. (original) A planar lightwave circuit comprising:

a substrate;

a plurality of waveguides arranged on the substrate; and

a distinct region on the substrate wherein at least a portion of the plurality of waveguides therein are modified relative to the plurality of waveguides outside the distinct region, the modifications including at least one of an expanded waveguide width of a waveguide, a gap within a waveguide and a lateral offset between a section of a waveguide within the distinct region and a section of the waveguide outside the distinct region.

35. (New) A method of fabricating a planar circuit utilizing the photolithographic mask set defined in claim 1, the method comprising:

(a) providing the photolithographic mask set;

(b) using the photolithographic mask set to expose at least part of a substrate;

(c) processing the exposed substrate to fabricate the planar circuit;

(d) analyzing the fabricated planar circuit; and

(e) determining an optimized planar circuit in dependence upon the analysis.